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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,610	03/10/2004	Sun-Young Kim	8750-059	6183

7590 12/29/2004

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/798,610	KIM, SUN-YOUNG	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-19* is/are allowed.

6)☒ Claim(s) *20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/10/2004 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 20 and 24** are rejected under 35 U.S.C. 102(b) as being anticipated by Haskell U.S. Patent 4,495,025.

Haskell discloses in Figures 1's, particularly Fig. 1K, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 20**, Haskell discloses a semiconductor device, comprising:

a semiconductor substrate (14) having a first region (20), a second region (18) spaced apart from the first region, and a border region (generally defined by groove 34) between the first and second regions;

a first trench region (groove 32) formed in the first region to define a first active region;

a second trench region (30) formed in the second region to define a second active region; and

a border trench region (34) formed in the border region, the border trench region deeper than the first and second trench regions.

Referring to **claim 24**, Haskell further discloses isolation layers (38,40) that fill the first trench region, the second trench region, and the border trench region.

3. **Claims 20-21 and 23-24** are rejected under 35 U.S.C. 102(e) as being anticipated by Saito U.S. Patent 6,596,608.

Saito discloses in Figures 1 through 14's, particularly Fig. 14D, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 20**, Saito discloses a semiconductor device, comprising:

a semiconductor substrate (1) having a first region (22, Fig. 1), a second region (20) spaced apart from the first region, and a border region (21) between the first and second regions;

a first trench region (generally referred to as 8c, Fig. 14D) formed in the first region to define a first active region;

a second trench region (generally referred to as 8a) formed in the second region to define a second active region; and

a border trench region (generally referred to as 8b) formed in the border region, the border trench region deeper than the first and second trench regions.

Referring to **claim 21**, Saito further discloses that the first region comprises a peripheral circuit region and the second region comprises a flash memory cell array region (column 8, lines 57-60).

Referring to **claim 23**, Saito further discloses that the first trench region (8c) is deeper than the second trench region (8a, best seen in Figs. 8D and 9D).

Referring to **claim 24**, Saito further discloses isolation layers (8) that fill the first trench region, the second trench region, and the border trench region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 22 is rejected under 35 U.S.C. §103(a) as being unpatentable over Saito as applied to claim 20 above, and further in view of Hwang U.S. Patent 5,576,226 or Jeong U.S. Patent 6,780,715.

Saito discloses a semiconductor device as claimed and as detailed above and further discloses a first gate insulating layer (32) and a first lower gate electrode pattern (10b) that are sequentially stacked on the first active region, and a second gate insulating layer (3) and a second lower gate electrode pattern (4) that are sequentially stacked on the second active region, the second gate insulating layer having a thickness of about 10 nm (column 10, last paragraph).

However, Saito fails to disclose that the second gate insulating layer having a different thickness from the first gate insulating layer.

Hwang, in also disclosing a semiconductor device having a peripheral circuit area including a first gate insulating layer and a memory area including a second gate insulating layer, teaches in column 4, lines 35-40, that thinner first gate insulating oxide layer makes the driving current increase, obtaining high-speed operation thereby, while the relatively thicker gate oxide layer in the cell area makes the defect density reduce, improving the reliability, thus teaching that by forming the second gate insulating layer having a different thickness from the first gate insulating layer, the mentioned advantages achieved; or Jeong, in also disclosing a semiconductor device having a peripheral circuit area (logic area) including a first gate insulating layer and a memory area including a second gate insulating layer, teaches in column 1, lines 44-54, that for the logic part to have high performance while the memory part to have reliability, a gate oxide film with different thickness is applied to each of the logic region and the memory region of the device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the Saito's semiconductor device so that the second gate insulating layer having a different thickness from the first gate insulating layer. One would have been motivated to make such a modification in view of the teachings in either Hwang or Jeong that the first and second gate insulating layers with different thickness offer advantages such as high performance and reliability as mentioned above.

Allowable Subject Matter

5. Claims 1-19 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach or render obvious a method with **all** exclusive limitations as recited in claims 1 and 12, characterized in removing the gate etching stopper layer pattern to expose the first lower gate conductive layer pattern, forming first and second trench mask patterns on respective portions of the first and second lower gate conductive layer patterns, etching the first and second lower gate conductive layer patterns and the first and second gate insulating layer patterns using the first and second trench mask patterns as etching masks to form first and second lower gate electrode patterns below the first and second trench mask patterns, respectively, the semiconductor substrate in the border region being etched during the etching process of the first and second lower gate conductive layer patterns to generate a groove region in the border region, and etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form trench regions, the trench region in the border region being formed to be deeper than the trench regions in the first and second regions.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
December 24, 2004